REMARKS/ARGUMENTS

This case has been carefully reviewed and analyzed in view of the Official Action dated 20 May 2004. Responsive to the rejections made by the Examiner in the Official Action, Claims 1, 4-6, 8-10, 12, 14 and 16 have been amended, Claim 15 has been canceled and Claims 17-22 have been appended for prosecution. The presently pending Claims 1, 4-6, 8-12, 14 and 16-22 now more clearly recite the inventive elements which form the invention of the subject Patent Application.

In the Official Action, the Examiner rejected Claims 8-13 under 35 U.S.C. §102(e) as being anticipated by Adams, et al. (US Patent #6,380,978; hereinafter "Adams"). With regard to previously presented Claim 8, the Examiner found that the navigation module of the present invention is met by video buffer 42 as depicted in Fig. 3 of Adams, that the decoder of the present invention is met by de-interlacing stage 1 as depicted in Figs. 4-5 and described at column 9, lines 12+ of Adams, that the detection module of the present invention claimed is met by de-interlacing elements 70 and 80 as depicted in Fig. 4 of Adams and that the processing module of the present invention is met by video output processor 60 as illustrated in Fig. 4 of Adams.

With regard to previously presented Claim 9, the Examiner found that the first processing module for concatenating fields of an input data frame into a digital video frame and the second processing module for providing a digital video frame that is based on field segments based on adjacent field segments of the input data frame are met by FIFO memories 136, 138, 140 in combination with field assembly 150 of Adams.

With regard to previously presented Claim 10, the Examiner found that detection module element of the present invention that determines the type of processing to be

performed on the video frame based on a predetermined number of prior video frames is met by de-interlacing elements 70 and 80 of Adams. Further, the Examiner found that the predetermined number of video frames being three (3), as recited in previously presented Claim 11 of the subject Patent Application, is depicted in Fig. 5 of Adams.

The Examiner found that the method of previously presented Claim 12 of the subject Patent Application is disclosed by Adams, in that: the step of obtaining current video information from an input video signal is met by video data buffer 42 of Adams; the step of separating the input video signal into a plurality of video frames is depicted in Fig. 5 of Adams; the step of detecting if each video frame matches an entry in a predetermined table for specifying a processing type is met by de-interlacing elements 70 and 80 of Adams; and, the step of generating a filtered video frame in response to information contained in the predetermined table is met by video output module 60 of Adams, which generates a video signal to be displayed in response to information contained in the FIFO and addressing and sequencing module 90.

The Examiner referred to the rejections of previously presented Claim 8 at (c) and (d) in rejecting previously presented Claim 13.

In the Official Action, the Examiner rejected Claims 1, 2, 4-6 and 16 under 35 U.S.C. §103(a) as being unpatentable over Adams. In rejecting previously presented Claim 1, the Examiner found that the navigation unit of the present invention is met by video data buffer 42 of Adams, that the decoder of the present invention is met by the de-interlacing stage 1 of Adams and that the processing unit of the present invention is met by the video output processor 60 of Adams. With regard to the detection unit of the present invention as previously claimed, whereby a first type of processing is specified

when a match of an entry of the look-up table by a frame and a second type of processing is specified when a match is not found, the Examiner stated that de-interlacing stage 70 of Adams performs progressive frame sequence detection and field difference processing, and de-interlacing stage 80 performs vertical frequency detection, signal reversal detection and diagonal feature detection, that SDRAM controller controls data passing to and from SDRAM memory and that the process of detecting current, last and next fields and processing either field difference processing or frequency detection. The Examiner then found that it would have been obvious to modify Adams to perform frame by frame processing as opposed to the field by field processing of Adams to make processing easier and/or faster.

With regard to previously presented Claim 2, the Examiner found that the isolation of the video signal from a DVD is met by DVD Media Transport 22 of Adams.

The Examiner found that invention as recited in previously presented Claim 4, wherein the each frame is generated from the field data of a predetermined number of prior frames, is met by de-interlacing stages 70 and 80 of Adams. The Examiner found further that the limitation of previously presented Claim 5, wherein the predetermined number of prior frames is three (3) is depicted in Fig. 5 of Adams.

Regarding the present invention as recited in previously presented Claim 6, the Examiner found that providing a frame that is a concatenation of fields of an input data frame or contains field values based on the values of fields of adjacent frames as specified by the look-up table is met by FIFOs 136, 138, 140 in combination with field assembly 150 outputting frame 152 of Adams.

The Examiner referred to the rejections of previously presented Claim 1 at (d) in rejecting previously presented Claim 16.

In the Official Action, the Examiner rejected Claims 14 and 15 under 35 U.S.C. §103(a) as being unpatentable over Callahan (US Patent #6,380,985). With regard to Claim 14, the Examiner found that Callahan discloses separating a video image frame into its component fields by step 100 of Fig.3, determining which of the component fields is the first component field by step 102 of Fig.3, and generating a combined video image frame signal based only on said first component field by step 106 of Fig.3. The Examiner found that limitation of the component field being a plurality of pixel lines is disclosed by Fig. 8 and column 11, lines 27-37 of Callahan.

Regarding the method step of previously presented Claim 14, whereby the second component field is discarded, the Examiner stated the Callahan illustrates the removal of a scan line and filtering the remaining field of scan lines. As noted by the Examiner, Callahan teaches that "It is immaterial which field is eliminated, and either one can be discarded" in column 4, lines 47-50. The Examiner concluded that the fact that either field can be discarded shows the flexibility of the methods of Callahan and that it would therefore be a matter of design choice to modify the system of Callahan to discard the second component field of each video frame.

With regard to the present invention as recited in previously presented Claim 15, the Examiner found that the method step of generating a pixel line having a value of the average of each adjacent pair of pixel lines and the method step of providing the generated pixel line between corresponding adjacent pairs of pixel lines are met by the disclosure of Callahan at column 5, lines 8-22.

In response to Applicant's arguments of 29 March 2004, the Examiner disagreed with assertions that Adams shows neither matching entries in a predetermined look-up table nor detecting matches of entries in a predetermined look-up table. The Examiner stated that "Given reasonably broad interpretation, a look-up table is a memory or storage device such as the SDRAM disclosed in the reference of Adams et al." The Examiner further stated that the SDRAM controller controls data in and out of SDRAM and that the de-interlacing stages 70 of Adams performs the functions of progressive frame sequence detection and field difference processing and that the de-interlacing stage 80 of Adams performs vertical frequency detection, signal reversal detection and diagonal feature detection. The Examiner further stated that Adams teaches FIFO addressing and sequencing 90 is attached to the de-interlacing stages and the Adams discloses detection of the current, last and next fields and processing either field by difference processing or frequency detection.

The Examiner also disagreed with Applicant's argument that Callahan discloses resizing a video signal and does not disclose a method for removing artifacts from a video signal. The Examiner stated that the system of Callahan is not limited to resizing only and may be applied to anti-flickering as well. The Examiner maintained that "applicant's argument that Callahan's teaching of discarding any field is immaterial, is definitely applicable and renders obvious the claimed invention of claim 14."

With regard to Applicant's arguments that none of the original lines are used after the resizing operation disclosed by Callahan, the Examiner cited column 4, lines 47-55 thereof, which states, "It is immaterial which field is eliminated, and either one can be

discarded." The Examiner concluded that some original lines must be used with one field is eliminated.

Prior to addressing the cited references with respect to Applicant's system and method for de-interlacing a video signal, it is believed beneficial to first briefly describe the structures and procedures executed thereon in light of the currently amended Claims, the Specification and the Drawings. The present invention provides means by which a digital video data stream, such as that provided by a DVD playback system, may be processed to be presented on a progressive display device.

As is known in the art, a disparity exists in display technologies, and not all video signals are displayable on a given display device. A fundamental difference in display devices, as is well known, is in the use of interlacing, wherein a video frame is composed of alternating field lines of a series of fields. A display device that is designed to display an interlaced video signal, such as a television set conforming to NTSC standards, displays the fields one at a time in rapid succession so as to be unperceivable by the human senses. However, when an interlaced video signal is displayed on a progressive display device, such as a computer monitor, the fields are displayed simultaneously, thereby producing video imagery beset with undesirable artifacts. Such artifacts are well known in the art and include jagged edges at object interfaces and non-fluid motion of objects (e.g., flicker).

The system and method of the present invention removes or mitigates the artifacts by one of several processing techniques, which is selected by either user-selection, by retrieval of processing information directly from the video data, or by interpretation of the processing methods on previous frames. Moreover, as the processing of video data

generally involves high computational costs, the present invention operates in a fashion believed to be novel in the art so as to minimize the computational requirements during presentation of the video data on the display device.

As disclosed by the Specification of the subject Patent Application, the system of the present invention includes a navigation unit for isolating the video data from a digital data stream and a decoder to separate the isolated video data into video data frames. The system as now claimed further includes a detection unit that generates a look-up table prior to the processing of any video data frame. The look-up table entries are filled during an initialization procedure with a processing type associated with each video data frame. Subsequently, during the presentation of data, the look-up table is consulted to determine a processing procedure for the associated data frame and provides indication of the processing type to the claimed processing unit. The processing unit processes the data frame in accordance with the processing type indication provided thereto so as to produce a filtered video frame suitable for display on the progressive display device. Thus, the present invention, as now claimed, operates to provide run-time speed through a priori generation of a look-up table, i.e., identifying the image processing requirements of each video data frame prior to video presentation reduces the computational load during playback.

In certain cases, the processing type is not identified during the initialization phase and, as such, an entry indicative thereof cannot be entered into the look-up table. The present invention, in such cases, enters a null value, such as a zero (0), into the table and the type of processing for the associated frame may be derived by the disclosed bit-stream detection.

The present invention is adapted to separate video frame data into its component fields and process the individual fields for display. As the individual fields are to be presented in a predetermined temporal order, the present invention, as now claimed, identifies which field is the first field in the presentation order. If it is determined that the first field is that which is to be processed, the field lines of the second field are ignored and the first field is interpolated in a first manner to form a video data frame for display. If the second field is that which is to be processed, the field lines of the first frame are ignored and the second field is interpolated in a second manner to produce the video data frame.

As previously stated, the Claims of the subject Patent Application have been amended to more clearly recite the elements of the present invention. Claim 1 has been amended to recite that the detection unit includes "means for generating a look-up table prior to processing [the] plurality of frames for display" and "means for providing an indication of [the] processing type entry". Claim 1 has been further amended to recite that the processing unit is "responsive to said indication of said processing type entry for providing a filtered video frame".

Claim 4 has been amended to recite that "a third processing type entry induces execution of a third processing algorithm in said processing unit upon said indication thereof, said third processing algorithm producing said filtered video frame from field data of said each frame and a predetermined number of preceding frames."

Claim 5 has been amended to recite the case where "said predetermined number of preceding frames is three."

Claim 6 has been amended to recite "a second processing type entry induces execution of a second processing algorithm in said processing unit upon said indication thereof, said second processing algorithm producing said filtered video frame by concatenating said fields of said each frame.

Claim 8 has been amended to recite that the detection module includes "means for generating a look-up table prior to processing said plurality of frames for display" and having "means for providing an indication of said processing type entry corresponding to said each video frame from said look-up table", and having "means for user selection of processing type for said each video frame". Claim 8 has been amended further to recite that the processing module is "responsive to said indication of said processing type entry for providing a filtered video frame for display on a progressive display device".

Claim12 has been amended to include the method steps of "generating a look-up table having a plurality of processing type entries prior to processing said plurality of video frames, each of said processing type entries respectively storing an indication of a processing algorithm for processing field data of a corresponding one of said plurality of video frames", "retrieving one of said plurality of processing type entries corresponding to one of said plurality of video frames prior to the display thereof", and "processing said one of said video frames in accordance with said processing algorithm indicated by said corresponding processing type".

Claim 14 has been amended to recite that, "a first one of [the] component fields is associated with a display time preceding that of a second one of said component fields", "determining which of said component fields is said first component field", "selecting one of said first component field and said second component field of said video image

frame for processing to a filtered video frame", "setting a first pixel line of said filtered video frame to a first pixel line of said component field selected", "setting said second pixel line of said filtered video frame to said first pixel line of said component field selected ... if said selected component field is said second component field", "generating a pixel line having pixel values equal to an average of corresponding pixels in each adjacent pair of pixel lines of said selected component field", and "inserting said generated pixel line between said corresponding adjacent pair of pixel lines of said filtered video frame except said first pixel line and said second pixel line if said selected component field is said second component field".

Claim16 has been amended to recite that the detection unit may include "means for user selection of processing type for said each frame, said user selection overriding said processing type entry thereof".

Claim 17 has been inserted to recite that "a first processing type entry induces execution of a first processing algorithm in said processing unit upon said indication thereof, said first processing algorithm producing said filtered video frame from a sum of scaled field data of adjacent field segments of said each frame".

Claim 18 has been added to recite that the third processing type entry may be "a null entry into said look-up table, said indication thereof corresponding to no predetermined processing type associated with said corresponding frame".

Claim 19 has been added to recite that the detection unit of currently amended Claim 1 may include "means for determining the type of processing to be performed on said each frame based on field data said each frame and a predetermined number of preceding frames".

Claim 20 has been inserted to recite that the video frame processing step of Claim 12 may include the step of "concatenating fields corresponding to each frame when said processing type entry indicates a first processing algorithm".

Claim 21 has been added to recite that the video frame processing step of Claim 12 may include the steps of "multiplying pixel values of each field line in each of said plurality of video frames by a corresponding scalar value", and "summing adjacent scaled field lines" when said processing type entry indicates a second processing algorithm.

Claim 22 has been inserted to recite that the video signal processing method of Claim 12 may include the step of "overriding said processing type entry in said look-up table for any of said plurality of video frames with a user selection of processing type".

In the rejection of Claims, as previously presented, the Examiner defined a look-up table as "a memory or storage device such as the SDRAM disclosed in the reference of Adams et al." It is respectfully submitted that this interpretation is overly broad and that the look-up table as implemented by the present invention, as now claimed, cannot be classified in such manner. Whereas a look-up table may be *stored* in a memory device such as an SDRAM, it is actually a *data structure* forming, in the case of the present invention, a relational database. The present invention accesses the look-up table with a key, such as the disclosed data frame time, and the look-up table returns a value, such as the processing type, associated with the key. It is submitted, respectfully, that equating the data structure with memory hardware by which it may be stored appears to be an attempt to fit the disclosure of Adams via the application of hindsight to the invention of the subject Patent Application. Moreover, Adams does not show, or even suggest, that the processing of a video frame proceeds "responsive to said indication of said processing

type entry for providing a filtered video frame" as now recited in Claim 1 of the subject Patent Application in that the SDRAM of Adams does not provide "an indication of said processing type entry" to any processing means disclosed thereby.

Also, in rejecting previously submitted Claims, the Examiner stated that the detection unit of the present invention having a first type of processing specified when a match of an entry of the look-up table by a frame and a second type of processing specified when a match is not found is obvious in view of Adams' de-interlacing stage 70 performing progressive frame sequence detection and field difference processing, and de-interlacing stage 80 performing vertical frequency detection, signal reversal detection and diagonal feature detection, coupled with SDRAM controller controlling data passing to and from SDRAM memory and detecting current, last and next fields and processing either field difference processing or frequency detection based thereon. However, a look-up table, as implemented by the present invention and as now claimed, is absent from Adams. In fact, all frames presented to the invention of Adams are processed by *both* de-interlacing stage 70 *and* de-interlacing stage 80 at some point in the processing sequence. This configuration is a data pipeline structure well-known in the art and does not attempt to fulfill the function of a look-up table. The invention of the subject Patent Application provides an independent processing choice on a frame by frame basis, whereas the frames processed by the invention of Adams are ultimately processed identically.

All of the references cited by the Examiner fail to show, or even suggest, "means for generating a look-up table prior to processing [a] plurality of frames for display" or a method step of "generating a look-up table having a plurality of processing type entries prior to processing said plurality of video frames, each of said processing type entries

respectively storing an indication of a processing algorithm for processing field data of a corresponding one of said plurality of video frames" as implemented by the present invention, as now claimed. As such, the references fail to show each and every element recited in Independent Claims 1 and 8, and fail to show each and every method step of Independent Claim 12, the references cited cannot anticipate the invention of the subject Patent Application, as now claimed. Moreover, as discussed hereinabove, the use of a look-up table to provide "an indication of said processing type entry" to the processing unit which is "responsive to said indication of said processing type entry for providing a filtered video frame" is not disclosed, suggested, or even considered by the references cited and it is believed that the present invention, as now claimed, is not made obvious thereby. Thus, as Independent Claims 1, 8 and 12 are now believed to be in condition for allowance, and Dependent Claims 2, 4-6, and 16-19 are ultimately dependent from Claim 1, Dependent Claims 10 and 11 are ultimately dependent from Claim 8, and Dependent Claims 21 and 22 are ultimately dependent from Claim 12, the Dependent Claims are also believed to be allowable.

In rejecting original Claim 14, the Examiner stated that Callahan teaches that "It is immaterial which field is eliminated, and either one can be discarded" concluding therefrom that as either field can be discarded, Callahan shows flexibility of its disclosed methods and that it would therefore be a matter of design choice to modify the system of Callahan to discard the second component field of each video frame. The invention of the subject Patent Application, however, requires the identification of the fields so that applicable processing may be applied. That is to say, for example, when the field is to be presented as the later of the two fields in a frame, the first pixel line of the field is

inserted as the first *two (2)* pixel lines of the processed frame. When the field is the earlier of the two, the first two pixel lines of the processed frame, prior to interpolation, may correspond to the first two pixel lines of the field. Once the first pixel lines have been inserted into the processed frame, the disclosed interpolation process is executed. This distinction is reflected in amended Claim 14 in the steps "a first one of said component fields is associated with a display time preceding that of a second one of said component fields", "determining which of said component fields is said first component field", "selecting one of said first component field and said second component field of said video image frame for processing to a filtered video frame", "setting a first pixel line of said filtered video frame to a first pixel line of said component field selected", "setting said second pixel line of said filtered video frame to said first pixel line of said component field selected ... if said selected component field is said second component field", "generating a pixel line having pixel values equal to an average of corresponding pixels in each adjacent pair of pixel lines of said selected component field", and "inserting said generated pixel line between said corresponding adjacent pair of pixel lines of said filtered video frame except said first pixel line and said second pixel line if said selected component field is said second component field". As noted by the Examiner, Callahan treats both fields equally. Thus, Callahan actually *teaches away* from processing the individual fields by respectively performing different processing thereon. Thus, it is believed that the invention of the subject Patent Application, as recited in amended Claim 14, cannot be made obvious by Callahan.

In view of the foregoing amendments and remarks, Applicant believes that the subject Patent Application is in condition for allowance and such action is respectfully requested.

Respectfully submitted,
For: ROSENBERG, KLEIN & LEE

Morton J. Rosenberg
Registration #26, 049

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